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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,245	02/17/2004	Chang-hyun Park	5649-1200	9654

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EXAMINER	
PHAM, THANH V	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,245	PARK ET AL.	
	Examiner	Art Unit	
	Thanh V. Pham	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 10-15* is/are rejected.

7)☒ Claim(s) *5-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Methods of Fabricating MOS Field Effect Transistors with Pocket Regions using Implant Blocking Pattern.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-2, 10, and 13-15 are rejected under 35 U.S.C. 102(a) as being anticipated by Hook et al. US 6,489,223 B1.

Re claim 1, the Hook et al. reference discloses a method of fabricating a MOSFET with pocket regions using angled implant process, comprising:

forming a gate electrode layer 12a on a semiconductor substrate 10;

forming lightly doped drain regions 44/60 in the semiconductor substrate adjacent the gate electrode layer, figs 3a and 4a;

forming a blocking pattern 18/19 on the semiconductor substrate, the blocking pattern being adjacent and spaced apart from the gate electrode layer a predetermined distance and exposing portions of the semiconductor substrate adjacent sidewalls of the gate electrode layer, fig. 2c;

forming pocket regions 46/58 in the semiconductor substrate by implanting impurity ions using the gate electrode layer and the blocking pattern as an ion implantation mask, col. 7, lines 25-26.

Re claim 2, the method further comprises: removing the blocking pattern; forming spacers 50/52 on the sidewalls of the gate electrode layer; and implanting impurity ions using the gate electrode layer having the spacers as an ion implantation mask to form deep source/drain regions 54/56 in the semiconductor substrate, col. 6, lines 42-45.

Re claims 10 and 13, the area of the pocket regions is controlled by adjusting a thickness of the blocking pattern and the distance between the sidewalls of the gate electrode layer and the blocking pattern, wherein the blocking pattern has a thickness h,

the pocket regions have a width d – [(l + d) / 2], the impurity ions are implanted at a tilt angle theta1, and an expected range of R_p (which depends on the power/time of the implantation and the substrate material, the formula as of claim 13 can be obtained), col. 4, line 42 to col. 5, line 23 and col. 5, line 50 to col. 6, line 12 and col. 6, lines 35-41.

Re claims 14-15, the forming LDD is followed by forming pocket regions or the forming pocket regions is followed by forming LDD, col. 6, line 42 to col. 7, line 50.

5. Claims 1-3, 10 and 14-15 are rejected under 35 U.S.C. 102(a) as being anticipated by Lenoble et al. US 6,806,156 B2.

Re claim 1, the Lenoble et al. reference discloses a method of fabricating a MOSFET with pocket regions, comprising:

forming a gate electrode layer GR on a semiconductor substrate ZA;

forming lightly doped drain regions LDD in the semiconductor substrate adjacent the gate electrode layer;

forming a blocking pattern RS on the semiconductor substrate, the blocking pattern being adjacent and spaced apart from the gate electrode layer a predetermined distance and exposing portions of the semiconductor substrate adjacent sidewalls of the gate electrode layer;

forming pocket regions PK in the semiconductor substrate by implanting impurity ions using the gate electrode layer and the blocking pattern as an ion implantation mask, fig. 2.

Re claim 2, the method further comprises: removing the blocking pattern; forming spacers on the sidewalls of the gate electrode layer; and implanting impurity ions using the gate electrode layer having the spacers as an ion implantation mask to form deep source/drain regions in the semiconductor substrate, figs. 3-4.

Re claim 3, the semiconductor substrate is a silicon substrate, col. 4, lines 15-16.

Re claims 10 and 13, the area of the pocket regions is controlled by adjusting a thickness of the blocking pattern and the distance between the sidewalls of the gate electrode layer and the blocking pattern; depending on the power/time of the implantation and the substrate material, the formula as of claim 13 can be obtained, col. 4, lines 33-59.

Re claims 14-15, the forming LDD is followed by forming pocket regions or the forming pocket regions is followed by forming LDD, col. 4, lines 60-67.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3-4, 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hook et al. as applied to claims 1-2, 10, and 13-15 above, and further in view of Takamura US 6,551,871 B1 and Kim et al. US Pub. No. 2002/0081795 A1.

The Hook et al. reference discloses substantially all of the instant invention wherein "either photoresist or hard mask can be used to form the barrier" (col. 7, lines 50-51) but lacks showing the material of the substrate and the gate electrode, the step of forming silicide after forming the source/drain, LDD and pocket regions.

The Takamura et al. reference discloses a typical FET in silicon (re claim 3), a gate electrode composed of a conducting material, such as conductive material or polysilicon (re claim 4), col. 4, lines 11-34 and fabricating a silicide layer after forming the source/drain, LDD and pocket regions col. 8, lines52-55. "the ion implantation is preferably performed with a mask having an opening only above the ... region so that the ... impurities are implanted only in the silicon film in the ... region. The mask may be a resist mask formed by photolithography or a so-called hard mask made of an insulating film (e.g., a silicon oxide film, a silicon nitride film or the like", col. 5, lines 27-33.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of Hook et al. with the silicidation of Takamura because the silicidation of Takamura would complete the FET formation of Hook et al.

8. Claims 1, 10, 12 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in combination with Handa et al. US Pub. No. 2004/0087095 A1 and/or Eikyu US Pub. No. 2003/0220770 A1.

Re claim 1, the applicant's admitted prior art reference discloses a method of fabricating a MOSFET with pocket regions, comprising:

forming a gate electrode layer 4 (of polysilicon, re claim 4) on a semiconductor substrate 1 (of silicon, re claim 3);

forming lightly doped drain regions 7 in the semiconductor substrate adjacent the gate electrode layer;

forming a blocking pattern 8 on the semiconductor substrate, the blocking pattern **not** being adjacent and spaced apart from the gate electrode layer a predetermined distance and exposing portions of the semiconductor substrate adjacent sidewalls of the gate electrode layer;

forming pocket regions 11 in the semiconductor substrate by implanting impurity ions using the gate electrode layer and the blocking pattern as an ion implantation mask.

The Handa et al. reference teaches in both prior art and its invention the formation of a hard mask 11/21/31/54 as the blocking pattern being adjacent and spaced apart from the gate electrode layer a predetermined distance and exposing portions of the semiconductor substrate adjacent sidewalls of the gate electrode layer for pocket implantation, [0074]. Re claim 10, the area of the pocket regions is controlled by adjusting a thickness of the blocking pattern and the distance between the sidewalls of the gate electrode layer and the blocking pattern, [0013]. Re claim 12, forming a blocking pattern 54 on the semiconductor substrate comprises forming a plurality of blocking layers 50/51 of figs. 7. Re claims 14-15, "the implantation of these pockets PK may be carried out before or after implantation of the zones LDD", [0074].

The Eikyu reference discloses design rule generating system related to a process of making a MOSFET, [0036] – [0042] and figs. 9-12, wherein the mask 35 is used for the oblique implantation to form pocket regions and also LDD, [0038].

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the applicant's admitted prior art with the blocking pattern as taught by Handa et al. and/or Eikyu because the blocking pattern of Handa et al. and/or Eikyu would provide the forming pocket regions of applicant's admitted prior art with "the direction of ion implantation being set closer to the horizontal direction" (Handa et al. 's [0012] or "to set the minimum shadowing margin within the range in which the electric characteristics of the MOS transistor are not deteriorated", Eikyu's [0041]).

Allowable Subject Matter

9. Claims 5-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: the cited prior art, individually or in combination, does not disclose or suggest all of the claimed elements in the present application wherein a photoresist pattern is formed on the two blocking layer to be spaced apart from the sidewalls of the gate electrode layer by a predetermined distance to expose portion of the second blocking layer between the pattern and the sidewalls of the gate electrode and a portion of the second blocking layer over the gate electrode layer in the context of claims 1 and 5.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-T (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVP

09/08/2005

George Fourson
Primary Examiner